

SOJ, TSOP, FP-BGA, TQFP Commercial Temp Industrial Temp

128K x 162Mb Asynchronous SRAM

8, 10, 12, 15ns 3.3V VDD Center VDD & Vss

Features

- Fast access time: 8, 10, 12, 15ns
- CMOS low power operation: 150/125/110/90 mA at min. cycle time.
- Single 3.3V ± 0.3V power supply
- · All inputs and outputs are TTL compatible
- · Byte control
- · Fully static operation
- Industrial Temperature Option: -40° to 85°C
- · Package line up
 - J: 400mil, 44 pin SOJ package
 - TP: 400mil, 44 pin TSOP Type II package
 - T: 10mm x 10mm, 44 pin TQFP
 - U: 6 mm x 8 mm Fine Pitch Ball Grid Array package

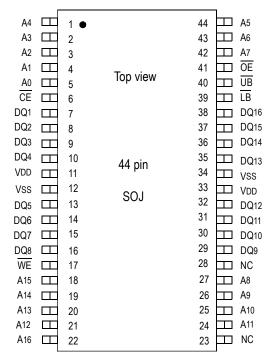
Description

The GS72116 is a high speed CMOS static RAM organized as 131,072-words by 16-bits. Static design eliminates the need for external clocks or timing strobes. Operating on a single 3.3V power supply and all inputs and outputs are TTL compatible. The GS72116 is available in a 6x8 mm Fine Pitch BGA package, a 10x10 mmTQFP package, as well as in 400 mil SOJ and 400 mil TSOP Type-II packages.

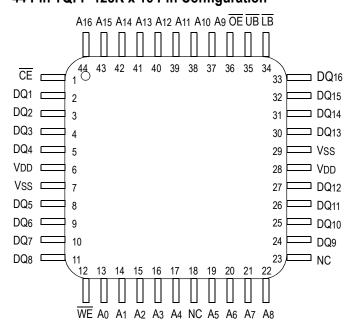
Pin Descriptions

Symbol	Description
A0 to A16	Address input
DQ1 to DQ16	Data input/output
CE	Chip enable input
LB	Lower byte enable input (DQ1 to DQ8)
ŪB	Upper byte enable input (DQ9 to DQ16)
WE	Write enable input
ŌĒ	Output enable input
VDD	+3.3V power supply
Vss	Ground
NC	No connect

SOJ 128K x 16 Pin Configuration



44 Pin TQFP 128K x 16 Pin Configuration



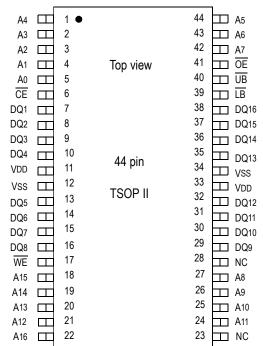


Fine Pitch BGA 128K x 16 Bump Configuration

	1	2	3	4	5	6
Α	LB	ŌE	A0	A 1	A2	NC
В	DQ16	ŪB	Аз	A4	CE	DQ1
С	DQ14	DQ15	A 5	A6	DQ2	DQ3
D	Vss	DQ13	NC	A 7	DQ4	VDD
Е	VDD	DQ12	NC	A16	DQ5	Vss
F	DQ11	DQ10	A8	A 9	DQ7	DQ6
G	DQ9	NC	A10	A11	WE	DQ8
Н	NC	A12	A13	A14	A15	NC

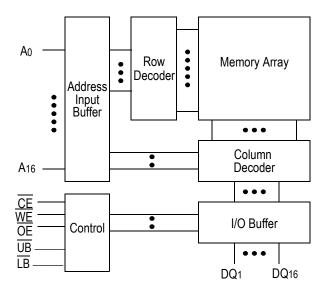
6mm x 8mm, 0.75mm Bump Pitch Top View

TSOP-II 128K x 16 Pin Configuration





Block Diagram



Truth Table

CE	ŌE	WE	LB	UB	DQ1 to DQ8 DQ9 to DQ16		VDD Current
Н	Х	Х	Х	Х	Not Selected	Not Selected	ISB1, ISB2
			L	L	Read	Read	
L	L	Н	L	Н	Read	High Z	
			Н	L	High Z	Read	
			L	L	Write	Write	lod
L	Х	L	L	Н	Write	Not Write, High Z	טטו
			Н	L	Not Write, High Z	Write	
L	Н	Н	Х	Х	High Z	High Z	
L	Х	Х	Н	Н	High Z	High Z	

Note: X: "H" or "L"



Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	Vdd	-0.5 to +4.6	V
Input Voltage	VIN	-0.5 to V _{DD} +0.5 (≤ 4.6V max.)	V
Output Voltage	Vouт	-0.5 to VDD+0.5 (≤ 4.6V max.)	V
Allowable power dissipation	PD	0.7	W
Storage temperature	Тѕтс	-55 to 150	°C

Note

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Тур	Max	Unit
Supply Voltage for -10/12/15	VDD	3.0	3.3	3.6	V
Supply Voltage for -8	VDD	3.135	3.3	3.6	V
Input High Voltage	ViH	2.0	-	VDD+0.3	V
Input Low Voltage	VIL	-0.3	-	0.8	V
Ambient Temperature, Commercial Range	TAc	0	-	70	°C
Ambient Temperature, Industrial Range	Tai	-40	-	85	°C

Note:

- 1. Input overshoot voltage should be less than VDD+2V and not exceed 20ns.
- 2. Input undershoot voltage should be greater than -2V and not exceed 20ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	CIN	VIN=0V	5	pF
Output Capacitance	Соит	Vout=0V	7	pF

Notes:

- 1. Tested at TA=25°C, f=1MHz
- 2. These parameters are sampled and are not 100% tested

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DC I/O Pin Characteristics

Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	lıL	Vin = 0 to VDD	-1uA	1uA
Output Leakage Current	lıo	Output High Z VOUT = 0 to VDD	-1uA	1uA
Output High Voltage	Vон	Iон = - 4mA	2.4	
Output Low Voltage	Vol	ILO = + 4mA		0.4V

Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C				-40 to 85°C			
Farameter	Symbol	rest conditions	8ns	10ns	12ns	15ns	10ns	12ns	15ns	
Operating Supply Current	loo	$\overline{\text{CE}} \leq \text{V}_{\text{IL}}$ All other inputs $\geq \text{V}_{\text{IH}} \text{ or } \leq \text{V}_{\text{IL}}$ Min. cycle time $\text{IOUT} = 0 \text{ mA}$	150mA	125mA	110mA	90mA	135mA	120mA	100mA	
Standby Current	ISB1	CE ≥ V _{IH} All other inputs ≥ V _{IH} or ≤V _{IL} Min. cycle time	55mA	50mA	45mA	40mA	60mA	55mA	50mA	
Standby Current	ISB2	$\overline{CE} \ge V_{DD} - 0.2V$ All other inputs $\ge V_{DD} - 0.2V \text{ or } \le 0.2V$	15mA				25mA			

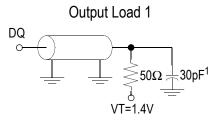


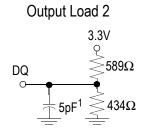
AC Test Conditions

Parameter	Conditions
Input high level	ViH=2.4V
Input low level	VIL=0.4V
Input rise time	tr=1V/ns
Input fall time	tf=1V/ns
Input reference level	1.4V
Output reference level	1.4V
Output load	Fig. 1& 2

Note:

- 1. Include scope and jig capacitance.
- Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted
- 3. Output load 2 for tLz, tHz, tOLz and tOHz.





AC Characteristics

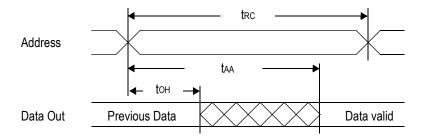


Read Cycle

Parameter	Cumbal	-	-8	-	10	-	12	-	15	Unit
Faranteter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Ullit
Read cycle time	t RC	8		10		12		15		ns
Address access time	taa		8		10		12		15	ns
Chip enable access time (CE)	t AC		8		10		12		15	ns
Byte enable access time (UB, LB)	t AB		3.5		4		5		6	ns
Output enable to output valid (OE)	toe		3.5		4		5		6	ns
Output hold from address change	tон	3		3		3		3		ns
Chip enable to output in low Z (CE)	t _{LZ} *	3		3		3		3		ns
Output enable to output in low Z (OE)	toLz*	0		0		0		0		ns
Byte enable to output in low Z (UB, LB)	t _{BLZ} *	0		0		0		0		ns
Chip disable to output in High Z (CE)	t _H z*		4		5		6		7	ns
Output disable to output in High Z (OE)	tonz*		3.5		4		5		6	ns
Byte disable to output in High Z (UB, LB)	t _{BHZ} *		3.5		4		5		6	ns

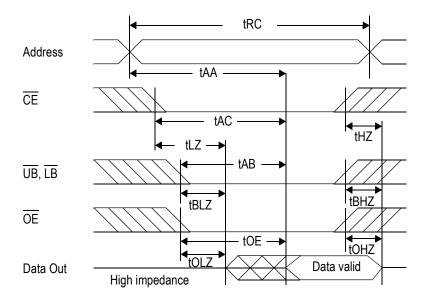
^{*} These parameters are sampled and are not 100% tested

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} and, or $\overline{LB} = V_{IL}$





Read Cycle 2: WE = V_{IH}



Write Cycle

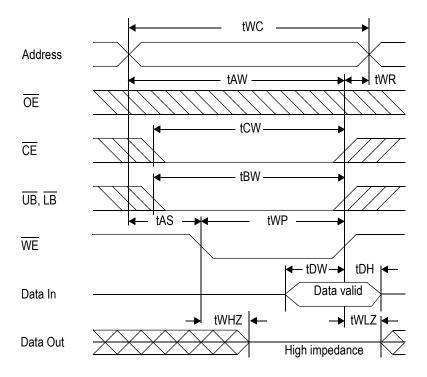
Parameter	Symbol	-	8	-1	10	-1	12	-1	15	Unit
Faianielei	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Offic
Write cycle time	tWC	8		10		12		15		ns
Address valid to end of write	tAW	5.5		7		8		10		ns
Chip enable to end of write	tCW	5.5		7		8		10		ns
Byte enable to end of write	tBW	5.5		7		8		10		ns
Data set up time	tDW	4		5		6		7		ns
Data hold time	tDH	0		0		0		0		ns
Write pulse width	tWP	5.5		7		8		10		ns
Address set up time	tAS	0		0		0		0		ns
Write recovery time (WE)	tWR	0		0		0		0		ns
Write recovery time (CE)	tWR1	0		0		0		0		ns
Output Low Z from end of write	tWLZ*	3		3		3		3		ns
Write to output in High Z	tWHZ*		3.5		4		5		6	ns

^{*} These parameters are sampled and are not 100% tested

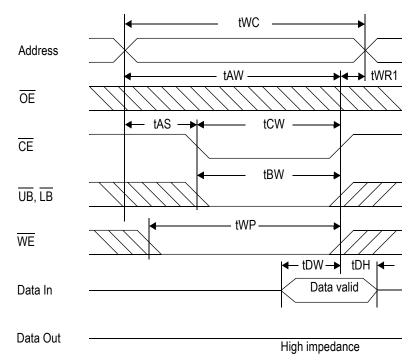
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Write Cycle 1: WE control

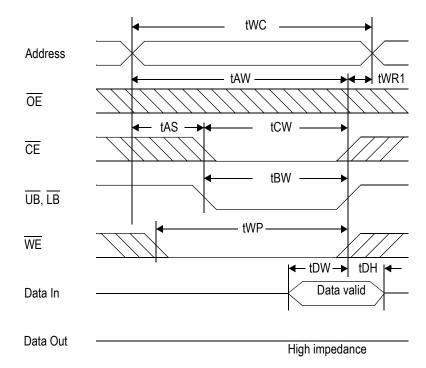


Write Cycle 2: CE control



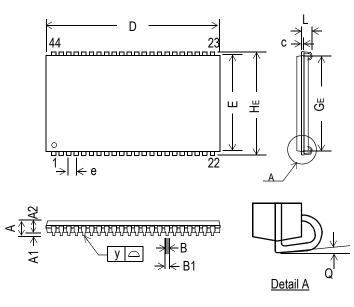


Write Cycle 3: UB, LB control





44 Pin, 400 mil SOJ



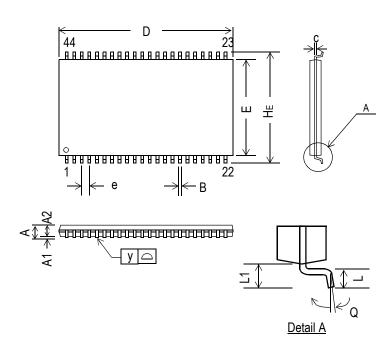
Symbol	Dime	nsion i	n inch	Dimension in mm					
Symbol	min	nom	max	min	nom	max			
А	-	-	0.148	-	-	3.759			
A1	0.025	-	-	0.635	-	-			
A2	0.105	0.110	0.115	2.667	2.794	2.921			
В	-	0.018	-	-	0.457	-			
B1	0.026	0.028	0.032	0.660	0.711	0.813			
С	-	0.008	-	-	0.203	-			
D	1.120	1.125	1.130	28.44	28.58	28.70			
Е	0.395	0.400	0.405	10.033	10.160	10.287			
е	-	0.05	-	-	1.27	-			
HE	0.435	0.440	0.445	11.049	11.176	11.303			
GE	0.360	0.370	0.380	9.144	9.398	9.652			
L	0.082	0.087	0.106	2.083	2.210	2.70			
у	-	-	0.004	-	-	0.102			
Q	0°	-	7°	0°	-	7°			

Note:

- 1. Dimension D& E do not include interlead flash
- Dimension B1 does not include dambar protrusion / intrusion



44 Pin, 400 mil TSOP-II



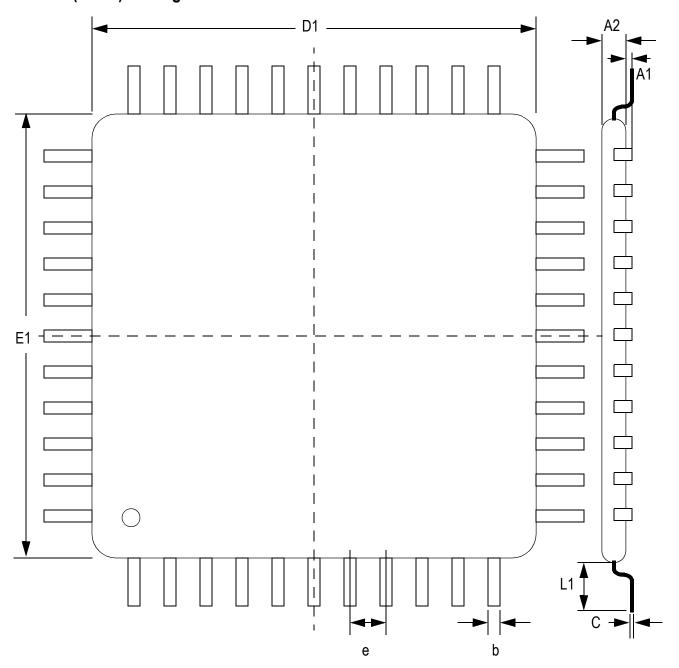
	Dimension in inch			Dimension in mm		
Symbol	min	nom	max	min	nom	max
Α	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
В	0.01	0.014	0.018	0.25	0.35	0.45
С	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
Е	0.396	0.400	0.404	10.06	10.16	10.26
е	-	0.031	-	-	0.80	-
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
у	-	-	0.004	-	-	0.10
Q	0°	-	5°	0°	-	5°

Note:

- 1. Dimension D& E do not include interlead flash
- 2. Dimension B does not include dambar protrusion / intrusion
- 3. Controlling dimension: mm



44 Pin TQFP (LQFP) Package

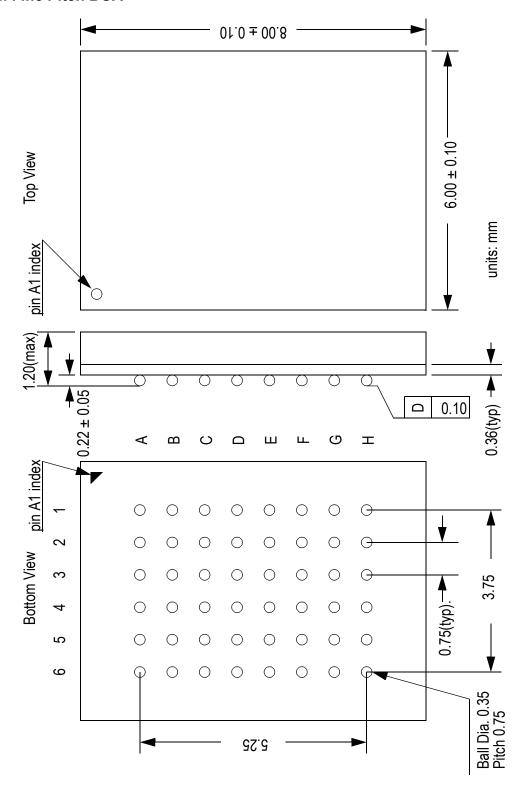


	Body Size		Lead Count	Standoff	Body Thickness	Lead Length	Lead Width	Lead Thickness	Lead Pitch
	E1	D1	Leau Count	A1	A2	L1	b	С	е
ſ	10	10	44	0.1	1.4	1.0	0.3	0.127	0.8

Units: mm



6mm x 8mm Fine Pitch BGA





Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS72116TP-8	400 mil TSOP-II	8 ns	Commercial	
GS72116TP-10	SS72116TP-10 400 mil TSOP-II		Commercial	
GS72116TP-12	400 mil TSOP-II	12 ns	Commercial	
GS72116TP-15	400 mil TSOP-II	15 ns	Commercial	
GS72116TP-8I	400 mil TSOP-II	8 ns	Industrial	
GS72116TP-10I	400 mil TSOP-II	10 ns	Industrial	
GS72116TP-12I	400 mil TSOP-II	12 ns	Industrial	
GS72116TP-15I	400 mil TSOP-II	15 ns	Industrial	
GS72116J-8	400 mil SOJ	8 ns	Commercial	
GS72116J-10	400 mil SOJ	10 ns	Commercial	
GS72116J-12	400 mil SOJ	12 ns	Commercial	
GS72116J-15	400 mil SOJ	15 ns	Commercial	
GS72116J-8I	400 mil SOJ	8 ns	Industrial	
GS72116J-10I	400 mil SOJ	10 ns	Industrial	
GS72116J-12I	400 mil SOJ	12 ns	Industrial	
GS72116J-15I	400 mil SOJ	15 ns	Industrial	
GS72116T-8	44 pin TQFP	8 ns	Commercial	
GS72116T-10	44 pin TQFP	10 ns	Commercial	
GS72116T-12	44 pin TQFP	12 ns	Commercial	
GS72116T-15	44 pin TQFP	15 ns	Commercial	
GS72116T-8I	44 pin TQFP	8 ns	Industrial	
GS72116T-10I	44 pin TQFP	10 ns	Industrial	
GS72116T-12I	44 pin TQFP	12 ns	Industrial	
GS72116T-15I	44 pin TQFP	15 ns	Industrial	



Ordering Information

Part Number*	Package	Access Time	Temp. Range	Status
GS72116U-8	Fine Pitch BGA	8 ns	Commercial	
GS72116U-10	Fine Pitch BGA	10 ns	Commercial	
GS72116U-12	Fine Pitch BGA	12 ns	Commercial	
GS72116U-15	Fine Pitch BGA	15 ns	Commercial	
GS72116U-8I	Fine Pitch BGA	8 ns	Industrial	
GS72116U-10I	Fine Pitch BGA	10 ns	Industrial	
GS72116U-12I	Fine Pitch BGA	12 ns	Industrial	
GS72116U-15I	Fine Pitch BGA	15 ns	Industrial	

^{*} Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. For example: GS72116TP-8T



Revision History

Rev. Code: Old; New	Types of Changes Format or Content	Page #/Revisions/Reason
GS721Rev1.05 10/19991/ 2000K;Rev 5 2/2000L	Format/Content	1. GSI Logo 2.